**CLAIM AMENDMENTS**

1. (currently amended) An edge sensitive detection circuit comprising:

a filter module operably coupled to receive an input logic signal, wherein the filter module produces, independent of a clock, a pulse signal in response to an edge of the input logic signal; and

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

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2. (previously amended) The edge sensitive detection circuit of claim 1, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.

3. (previously amended) The edge sensitive detection circuit of claim 2, wherein the second inverting logic element comprises an inverter and wherein the first

inverting logic element comprises at least one of an inverter and a NAND gate.

4. (original) The edge sensitive detection circuit of claim 1, wherein the filter module comprises:

a capacitor operably coupled to receive the input logic signal; and

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a gating circuit operably coupled to the capacitor, wherein the gating circuit generates the pulse signal, wherein the capacitor and an impedance of at least one element of the gating circuit are tuned based on at least one of rise time or fall time of the input logic signal.

5. (currently amended) The edge sensitive detection circuit of claim 4, wherein the gating circuit comprises:

an inverter, wherein an output of the inverter is operably coupled to a drive transistor of the soft latch module; and

a controlled impedance coupled to the capacitor and to a ground voltage, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor.

6. (original) The edge sensitive detection circuit of claim 1, wherein the input logic signal is at least one of: a reset signal, a power down signal, a power up signal, a standby signal, and a set signal.

7. (original) The edge sensitive detection circuit of claim 1 further comprises a second filter module operably coupled to receive a second input logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second input logic signal, and wherein the soft latch module latches the logic value in accordance with the second pulse signal.

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8. (original) The edge sensitive detection circuit of claim 7, wherein the second filter module comprises:

a second capacitor operably coupled to receive the second input logic signal; and

a second gating circuit operably coupled to the second capacitor, wherein the gating circuit generates the second pulse signal, wherein the second capacitor and an impedance of at least one element of the second gating circuit are tuned based on at least one of rise time or fall time of the second input logic signal.

9. (currently amended) A edge sensitive detection circuit comprises:

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an input gating device;

a processing module operably coupled to the input gating device, wherein the processing module utilizing operational instructions to process an input logic signal from the input gating device to produce a processed logic signal;

a filter module operably coupled to receive the processed logic signal, wherein the filter module produces, independent of a clock, a pulse signal in response to an edge of the processed logic signal; and

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a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

10. (previously amended) The edge sensitive detection circuit of claim 9 further comprises:

a second gating device that provides a second input logic signal to the processing module, wherein the processing module produces a second processed logic signal based on the second input logic signal;

a second filter module operably coupled to receive the second processed logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second processed logic signal; and

a second soft latch module operably coupled to receive the second pulse signal, wherein the second soft latch module latches a logic value in accordance with the second pulse signal.

11. (original) The edge sensitive detection circuit of claim 9, wherein the input gating device provides one of a plurality of input logic signals as the input logic signal.

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12. (previously amended) The edge sensitive detection circuit of claim 9, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.

13. (original) The edge sensitive detection circuit of claim 9, wherein the filter module comprises:

a capacitor operably coupled to receive the input logic signal; and

a gating circuit operably coupled to the capacitor, wherein the gating circuit generates the pulse signal, wherein the

capacitor and an impedance of at least one element of the gating circuit are tuned based on at least one of rise time or fall time of the input logic signal.

14. (currently amended) The edge sensitive detection circuit of claim 13, wherein the gating circuit comprises

an inverter, wherein an output of the inverter is operably coupled to a drive transistor of the soft latch module; and

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a controlled impedance coupled to the capacitor and to a ground voltage, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor.

15. (original) The edge sensitive detection circuit of claim 9, wherein the input logic signal comprises at least one of: a reset signal, a set signal, a power down signal, a power on signal, and a standby signal.

16. (original) The edge sensitive detection circuit of claim 9 further comprises a second filter module operably coupled to receive a second input logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second input logic signal, and wherein the soft latch module latches the logic value in accordance with the second pulse signal.

17. (currently amended) An edge sensitive detection circuit comprising:

a capacitor operably coupled to receive ~~the~~ an input logic signal;

a controlled impedance coupled to the capacitor, wherein the capacitor and an impedance of at least one element of a gating circuit are tuned based on at least one of rise time or fall time of the input logic signal;

an inverter, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor;

a drive transistor operably coupled to produce a pulse signal, independent of a clock signal, wherein an output of the inverter is operably coupled to the drive transistor; and

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

18. (previously amended) The edge sensitive detection circuit of claim 17, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.